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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,935	11/15/2001	William Lam	0007056-0022/P4777	2886

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EXAMINER
STEVENS, THOMAS H

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/990,935	LAM, WILLIAM
	Examiner	**Art Unit**	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _15 November 2001_.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-30_ is/are pending in the application.
  4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) _1-30_ is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on _15 November 2001_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  a) ☐ All b) ☐ Some * c) ☐ None of:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. _____.
    3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _1/22/03_.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-30 were examined.

Claim Rejections - 35 USC § 112

2.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 11-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Webster's dictionary defines **amortizing** as a method *"to liquidate (a debt) by installment payments or payment into a sinking fund; to write off an expenditure for (office equipment, for example) by prorating over a certain period"*. The examiner is unclear how amortizing pertains to the genre of electronics or science.

3.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4.   Claims 1, 11-29 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Webster's dictionary defines **amortizing** as a

method *"to liquidate (a debt) by installment payments or payment into a sinking fund; to*

write off an expenditure for (office equipment, for example) by prorating over a certain

period". The examiner is unclear how amortizing pertains to the genre of electronics or

science.

Claim Rejections - 35 USC § 103

5.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

> 1.   Determining the scope and contents of the prior art.
>
> 2.   Ascertaining the differences between the prior art and the claims at issue.
>
> 3.   Resolving the level of ordinary skill in the pertinent art.
>
> 4.   Considering objective evidence present in the application indicating
>
> obviousness or nonobviousness.

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 1-6,8-16,18-26, 28-30 are rejected under 35 U.S.C. 103(a) as being

unpatentable by Huang (U.S. Patent 5,095,454 (1992)) in view of Li (U.S. Patent

6,339,837 (2002)). Li teaches a method for verifying a digital circuit in a hardware

description language using a verification structure and a verification engine; but doesn't

teach critical paths or a single path after simulation. Huang teaches a digital simulation

method and apparatus which provides a critical path for timing analysis of digital

circuitry using a hybrid path tracing method. At the time of invention, it would have been

obvious to one of ordinary skill in the art to modify Li by way of Huang since the goal of

static timing analysis is to complete a timing verification in a single pass (Huang: column

1, lines 60-61).

Claim 1. A method for amortizing a critical path computations (Huang: abstract) in a

circuit comprising: unrolling (Li: column 5, lines 10-15) a data flow graph representing

(Huang: column 4, lines 30-49) said circuit into a plurality of clock cycles (Huang: claim

15, lines 40-46); and simulating said circuit in said plurality clock cycles on a computer

(Li: column 2, lines 23-30).

Claim 2.   The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Li: column

2, lines 23-30; Li: column 5, lines 10-15) wherein said step of simulating further

comprises: reducing a difference between said critical path and a shortest path in said

data flow graph (Huang: column 5, lines 45-55).

Claim 3.   The method of claim 2, (Huang: abstract; claim 15, lines 40-46; Huang:

column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15) wherein said

step of reducing further comprises: compacting one or more computations from plurality

of clock cycles in a processor.

Claim 4.   The method of claim 2, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15) wherein said step of unrolling further comprises: eliminating one or more flip-flops between (abstract: "eliminating blocked paths") one or more boundaries (Huang: columns 8 and 9, lines 67-68, lines 1-2) within said plurality of clock cycles (Huang: claim 15, lines 40-46).

Claim 5.   The method of claim 2, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15) wherein said step of unrolling further comprise: eliminating one or more latches between (Huang: abstract: "eliminating blocked paths") one more boundaries (Huang: columns 8 and 9, lines 67-68, lines 1-2) within said plurality of clock cycles (Huang: claim 15, lines 40-46).

Claim 6.   The method of claim 1, (Huang: abstract; claim 15, lines 40-46) wherein said computer has a plurality of processors.

Claim 8.   The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Li: column 2, lines 23-30; Li: column 5, lines 10-15) wherein said step of simulating further comprises: delaying evaluation of one or more logic elements (Huang: column 4, lines 42-46) within said plurality of clocks cycles (Huang: column 15, lines 40-46), thereby creating a timing slack (Huang: column 5, lines 25-30) for inter-processor communication (Li: column 7, lines 1-5).

Claim 9.   The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Li: column

2, lines 23-30; Li: column 5, lines 10-15) wherein said step of reducing further

comprises: using a first processor wherein said processor computes said critical path

(Huang: column 14, lines 10-21) and a non-critical path in a said plurality of clock cycles

(Huang: column 15, lines 40-46).

Claim 10.   The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Li: column

2, lines 23-30; Li: column 5, lines 10-15) further comprising: compacting said plurality of

clock cycles into a single clock cycle (Huang: column 15, lines 55-60).

Claim 11.   A critical path (Huang: column 14, lines 10-21) computation amortizer for

a circuit comprising: a data flow graph (Huang: column 4, lines 30-49) unroller (Li:

column 5, lines 10-15) configured to represent said circuit into a plurality of clock cycles

(Huang: claim 15, lines 40-46); and a simulator configured to simulate said circuit in said

plurality of clock cycles on a computer (Li: column 2, lines 23-30).

Claim 12.   The critical path (Huang: abstract) computation amortizer of claim 1,

(Huang: abstract; claim 15, lines 40-46; Li: column 2, lines 23-30; Li: column 5, lines 10-

15) wherein said simulator further comprises: a reducer configured to reduce a

difference between said critical path and said shortest path (Huang: column 5, lines 45-

55).

Claim 13.   The critical path (Huang: abstract) computation amortizer of claim 12,

(Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2,

lines 23-30; Li: column 5, lines 10-15) wherein said reducer further comprises: a

compactor configured to compact one or more computations from said plurality of clock

cycles in a processor.

Claim 14.   The critical path (Huang: abstract) computation amortizer of claim 12,

(Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2,

lines 23-30; Li: column 5, lines 10-15) wherein said unroller further comprises: an

eliminator configured to eliminate one or more flip-flops at one or more boundaries

within said plurality of clock cycles.

Claim 15.   The critical path computation amortizer of claim 12, (Huang: abstract;

claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li:

column 5, lines 10-15) wherein said unroller further comprises: an eliminator configured

to eliminate one or more latches between (Huang: abstract: "eliminating blocked paths")

one or more boundaries (Huang: columns 8 and 9, lines 67-68, lines 1-2) within said

plurality of clock cycles (Huang: claim 15, lines 40-46).

Claim 16.   The critical path (Huang: abstract) computation amortizer 11, (Huang:

abstract; claim 15, lines 40-46; Li: column 2, lines 23-30; Li: column 5, lines 10-15)

wherein said computer has a plurality of processors.

Claim 18.   The critical path (Huang: abstract) computation amortizer of claim 11,

(Huang: abstract; claim 15, lines 40-46; Li: column 2, lines 23-30; Li: column 5, lines 10-

15) wherein said simulator is further configured delay evaluation of one or more logic

elements (Huang: column 4, lines 42-46) in said plurality of clock cycles, (Huang:

column 15, lines 40-46) thereby creating a timing slack (Huang: column 5, lines 25-30)

for inter-processor communication (Li: column 7, lines 1-5).

Claim 19.   The critical path (Huang: abstract) computation amortizer of claim 13,

(Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2,

lines 23-30; Li: column 5, lines 10-15) wherein said reducer further comprises: a feed-

back configured to use a first processor wherein, said first processor computes said

critical path (Huang: column 14, lines 10-21) and a non-critical path in said plurality of

clock cycles (Huang: column 15, lines 40-46).

Claim 20.   The critical path (Huang: column 14, lines 10-21) computation amortizer

of claim 11, (Huang: column 14, lines 10-21; (Li: column 5, lines 10-15; Huang: claim

15, lines 40-46; Li: column 2, lines 23-30) further comprising: a scheduling compactor

configured to compact said plurality of clock cycles into a single clock cycle (Huang:

column 15, lines 55-60).

Claim 21.   A computer program product comprising: a computer usable medium

having computer readable code embodied therein configured to amortize a critical

computation (Huang: abstract) in a circuit, said computer program product comprising:

computer readable code configured to cause a computer to unroll (Li: column 5, lines

10-15 with figures 5 and 6) a data flow graph representing (Huang: column 4, lines 30-

49) said circuit into a plurality of clock cycles; and computer readable code configured to

cause a computer to simulate said circuit in said plurality of clock cycles on a computer

(Li: column 2, lines 23-30).

Claim 22.   The computer program product of claim 21, (Huang: abstract; Li: column

5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30) wherein said computer

readable code configured to cause a computer to simulate further comprises: computer

readable code configure to cause a computer to reduce a difference between said

critical path and said shortest path (Huang: column 5, lines 45-55).

Claim 23.   The computer program product of claim 22, (Huang: abstract; Li: column

5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30; Huang: column 5, lines 45-

55) wherein said computer readable code configured to cause a computer to unroll (Li:

column 5, lines 10-15) further comprises: computer readable code configured to cause

a computer to eliminate one or more flip-flops (abstract: "eliminating blocked paths") at

one more boundaries within said plurality of clock cycles (Huang: claim 15, lines 40-46).

Claim 24   The computer program product of claim 12, (Huang: abstract; claim 15,

lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines

10-15) wherein said computer readable code configured to cause a computer to unroll

further comprises (Li: column 5, lines 10-15): computer to eliminate one or more flip-

flops (abstract: "eliminating blocked paths") at one or more boundaries within said

plurality of clock cycles.

Claim 25.   The computer program product of claim 12, (Huang: abstract; claim 15,

lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines

10-15) wherein said computer readable code configured to cause a computer to unroll

further comprises (Li: column 5, lines 10-15): computer readable code configured to

cause a computer to eliminate one or more latches (Huang: abstract-- "eliminating

blocked paths") at one or more boundaries within said plurality of clock cycles.

Claim 26.   The computer program product of claim 21, (Huang: abstract; Li: column

5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30) wherein said computer has

a plurality of processors.

Claim 28.   The computer program product of claim 21, (Huang: abstract; Li: column

5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30) wherein said computer

readable code configured to cause a computer to simulate comprises: computer

readable code configured to cause a computer to delay evaluation (Huang: column 5,

lines 25-31) of one or more logic elements in said plurality of clock cycles (Huang:

column 15, lines 40-46), thereby creating a timing (Huang: column 5, lines 25-31) slack

for inter-processor communication.

Claim 29.   The computer program product of claim 20, (Huang: column 14, lines 10-

21; Huang: column 14, lines 10-21; (Li: column 5, lines 10-15; Huang: claim 15, lines

40-46; Li: column 2, lines 23-30; Huang: column 15, lines 55-60) wherein said computer

readable code configured to cause a computer to reduce further comprises: computer

readable code configured to cause a computer to use a first processor wherein said first

processor computes said critical path (Huang: column 14, lines 10-21) and a non-critical

path in said plurality of clock cycles(Huang: column 15, lines 40-46).

Claim 30.   The computer program product of claim 21, (Huang: abstract; Li: column

5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30) further comprising:

computer readable code configured to cause a computer to compact said plurality of

clock cycles (Huang: claim 15, lines 40-46) into a single clock cycles (Huang: column

15, lines 55-60).

8.   Claims 7,17 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable

by Huang (U.S. Patent 5,095,454 (1992)) in view of Abts et al., (U.S. Patent 6,856,950

(2005)) and in further view Li (U.S. Patent 6,339,837 (2002)). Li teaches a method for

verifying a digital circuit in a hardware description language using a verification structure

and a verification engine; but doesn't teach critical paths or a single path after

simulation or hardware support for barrier synchronization. Huang teaches a digital

simulation method and apparatus which provides a critical path for timing analysis of

digital circuitry using a hybrid path tracing method, while Abts et al., teaches a system

and method of verifying an electronic system with the ability construct a interconnection

network (Abts: column 49, lines 20-25) with hardware support for barrier

synchronization (Abts: column 49, lines 25-31).

At the time of invention, it would have been obvious to one of ordinary skill in the

art to modify Li by way of Huang and Abts et al., since the goal of static timing analysis

is to complete a timing verification in a single pass (Huang: column 1, lines 60-61) and

to have diagnostic system as well as a interprocess communication mechanism for

transforming stimulus from the diagnostic system to the hardware simulation for

transferring results from the hardware simulator to the diagnostic system (Abts: column

3, lines 2-5).

Clam 7.   The method of claim1, (Huang: abstract; claim 15, lines 40-46; Li: column

2, lines 23-30; Li: column 5, lines 10-15) wherein said computer has a plurality of

simulation processors, wherein said simulation processors include a communication

network interconnecting (Li: column 7, lines 1-5) said simulation processors for data

communication, (Li: column 7, lines 1-5) said simulation processors further including a

synchronization network (Abts: column 49, lines 21-27) interconnecting said simulation

processors for synchronizing execution (Abts: column 49, lines 21-27) there between.

Claim 17.   The critical path computation amortizer of claim 11, (Huang: column 14,

lines 10-21; Li: column 5, lines 10-15; Huang: claim 15, lines 40-46; Li: column 2, lines

23-30) wherein said computer has a plurality of simulation processors, wherein said

simulation processors include a communication network interconnecting (Li: column 7,

lines 1-5) said simulation processors for data communication, (Li: column 7, lines 1-5)

said simulation processors further including a synchronization network (Abts: column

49, lines 21-27) interconnecting said simulation processors for synchronization

execution (Abts: column 49, lines 21-27) there between.

Claim 27.   The computer program product of claim 21, (Huang: abstract; Li: column

5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30) wherein said computer has

a plurality of simulation processors, wherein said simulation processors include a

communication network (Li: column 7, lines 1-5) interconnecting said simulation

processors for data communication, said simulation processors further including a

synchronization network (Abts: column 49, lines 21-27) interconnecting said simulation

processors for synchronizing execution (Abts: column 49, lines 21-27) there between.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-

3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at
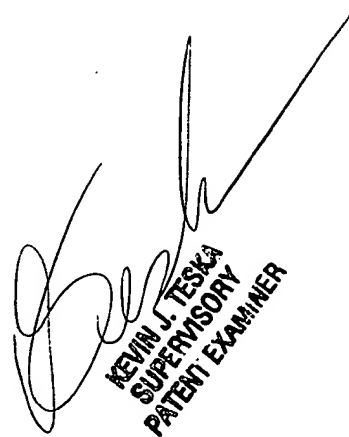
(571) 272-3716. Fax number is 571-273-3715.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

March 14, 2005

THS

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER